ABSTRACT OF THE DISCLOSURE

[1047] The present invention provides an efficient implementation of multiprecision arithmetic, such as for a microprocessor. For example, an implementation of multiprecision arithmetic is provided that eliminates condition codes, such as condition codes for a carry bit and a borrow bit, and eliminates an add-with-carry instruction for multiprecision addition and a subtract-with-borrow instruction for multiprecision subtraction. In one embodiment, a method includes separately performing a first one or more arithmetic operations and a second one or more arithmetic operations. The second arithmetic operations indicate if the first arithmetic operations cause a carry condition or if the first arithmetic operations cause a borrow condition. The one or more results of the first and second arithmetic operations are then provided. The first and second arithmetic operations can be executed in parallel on a microprocessor.